

What is claimed is:

1. A method for synchronizing the sampling rate of digital cells in an integrated services hub, comprising:

- 5 (a) extracting from the network connection a reference sampling rate representing the rate of sampling occurring at the end of the network connection opposite from the end connected to the integrated services hub; and
- (b) adjusting the sampling rate in the integrated services hub to about equal the reference sampling rate.

2. The method of claim 1 wherein the reference sampling rate is an embedded signal.

3. The method of claim 1 wherein the reference sampling rate is extrapolated from the arrival rate of incoming cells to the integrated services hub.

4. The method of claim 3 further comprising:
- monitoring the fill level of incoming cells received into an incoming cell buffer;
  - increasing the sampling rate in the integrated service hub in response to an increase in the fill level of the incoming cell buffer above the midpoint; and
  - decreasing the sampling rate in the integrated services hub in response to a decrease in the fill level of the incoming cell buffer below the midpoint.



5. The method of claim 4 further comprising using a voltage controlled oscillator to increase and decrease the sampling rate in the integrated services hub.

6. The method of claim 4 further comprising using a programmable frequency divider to  
5 increase and decrease the sampling rate in the integrated services hub.

7. The method of claim 6 wherein the programmable frequency divider is a baud rate generator.

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10. An apparatus for synchronizing the sampling rate of digital cells in an integrated services hub, comprising:

a sampling rate adjuster receiving a baseline clock signal and a reference sampling rate, the sampling rate adjuster adjusting the baseline clock signal to about equal the reference sampling rate and outputting a sampling rate signal equal to the adjusted baseline clock signal;

a central processing unit (CPU) communicating with and controlling the sampling rate adjuster;

a CODEC in communication with and receiving the sampling rate signal from the sampling rate adjuster; and

a feedback loop communicating the sampling rate signal from the sampling rate adjuster to the CPU.

11. The apparatus of claim 10 wherein the sampling rate adjuster is a voltage controlled oscillator.

12. The apparatus of claim 10 wherein the sampling rate adjuster is a programmable frequency divider.

13. The apparatus of claim 12 wherein the programmable frequency divider is a baud rate generator.

14. The apparatus of claim 10 wherein the reference sampling rate is the baseline clock signal.



19. The apparatus of claim 16 wherein the CPU calculates the reference sampling rate by monitoring the fill level of incoming cells received into an incoming cell buffer.